A Radiation-Tolerant Low-Power Transceiver Design for Reconfigurable Communications and Navigation Applications

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Advanced Engineering & Sciences

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Outline

The Low Power Transceiver (LPT)

The Radiation-Tolerant LPT

Applications of the LPT in Space

The Future

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Introduction to the Low-Power Transceiver (LPT)

❏ **LPT is a collection of interchangeable PC/104 hardware modules that form a software programmable platform for communication and navigation functions**

  ➢ **Simultaneously transmits and receives signals in multiple RF bands**
  ➢ **Simultaneously processes multiple data channels within each RF band**
  ➢ **Modular architecture allows flexibility of signal processing resources**

❏ **Primary goals**

  ➢ **Low power consumption**
  ➢ **Small form factor & reduced mass**
  ➢ **Reconfigurable signal processing**
  ➢ **Radiation tolerance**

❏ **Originally developed by NASA GSFC and ITT Industries, the LPT is evolving to meet the needs of numerous terrestrial, airborne, and space based users and missions**

Baseline LPT Configuration (3rd Generation)

- ❑ **Receiver**
  - ➢ **32 receiver channels**
    - • **28 channel GPS receivers (dual L1 or L1/L2)**
    - • **4 channels of dedicated communications**
      - – **NASA's Tracking and Data Relay Satellite System (TDRSS)**
      - – **NASA's Spaceflight Tracking and Data Network (STDN)**
      - – **Air Force Satellite Control Network (AFSCN)**
      - – **LPT-to-LPT crosslink**
  - ➢ **PSK, PM**
  - ➢ **Spread, non-spread**
  - ➢ **50 bps – 1 Mbps per channel**
  - ➢ **Integrated GPS solution software**

- ❑ **Transmitter**
  - ➢ **2 independent transmitter channels**
  - ➢ **BPSK, QPSK, OQPSK, linear PM**
  - ➢ **Spread, non-spread**
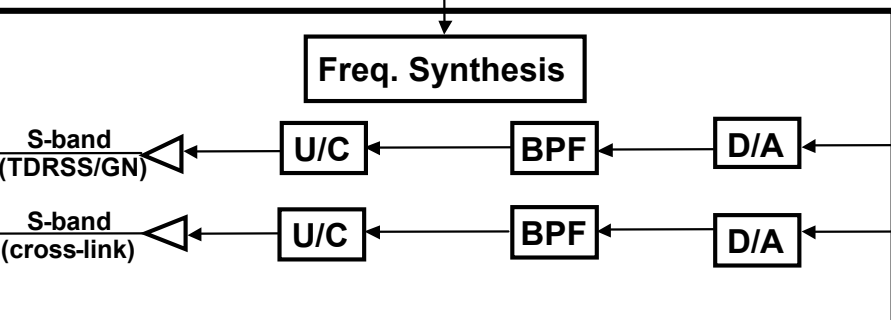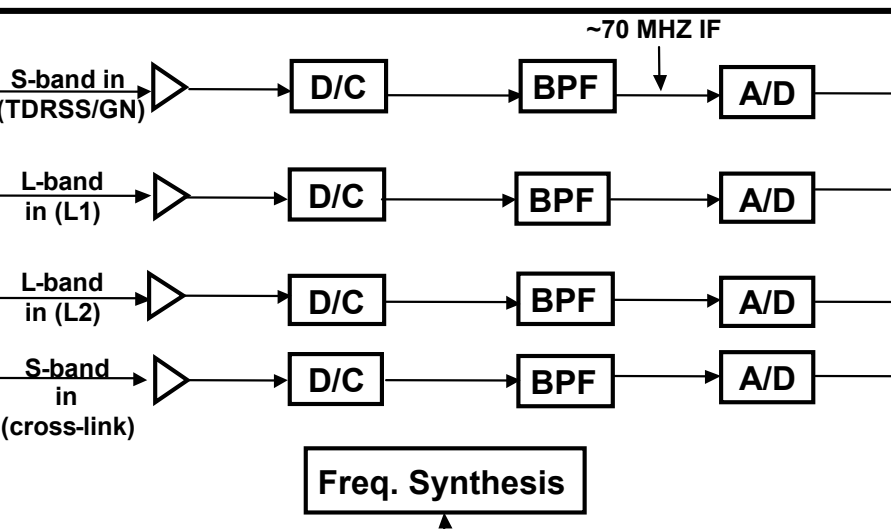 - ➢ **Up to 10 Mbps per channel**

- ❑ **Software Programmable Functions**
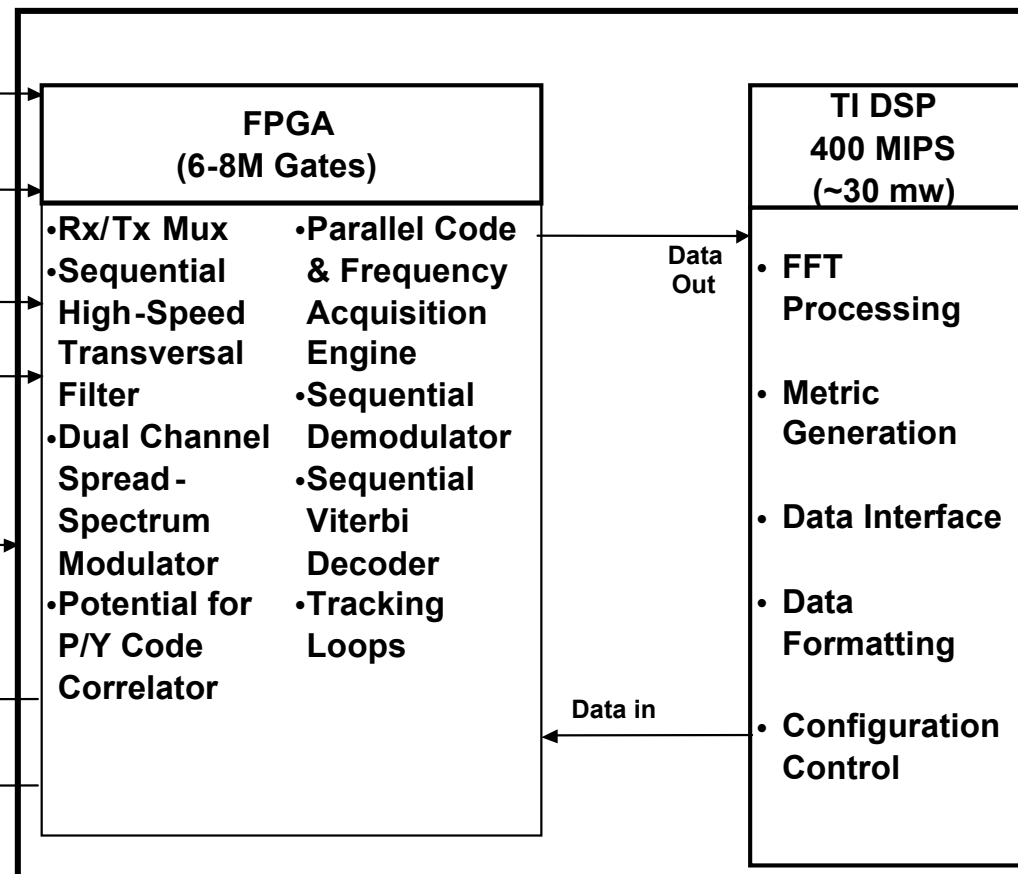 - ➢ **Functions tailored to application**

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3rd Generation LPT Architecture

RF Receive Card

~70 MHZ IF

S-band in (TDRSS/GN)	D/C → BPF → A/D	
L-band in (L1)	D/C → BPF → A/D	
L-band in (L2)	D/C → BPF → A/D	
S-band in (cross-link)	D/C → BPF → A/D	

Freq. Synthesis

Freq. Synthesis

FPGA (6-8M Gates)

- •Rx/Tx Mux
- •Sequential High-Speed Transversal Filter
- •Dual Channel Spread-Spectrum Modulator
- •Potential for P/Y Code Correlator

- •Parallel Code & Frequency Acquisition Engine
- •Sequential Demodulator
- •Sequential Viterbi Decoder
- •Tracking Loops

TI DSP 400 MIPS (~30 mw)

Data Out

- • FFT Processing
- • Metric Generation
- • Data Interface
- • Data Formatting
- • Configuration Control

Data in

S-band (TDRSS/GN)	U/C ← BPF ← D/A
S-band (cross-link)	U/C ← BPF ← D/A

RF Transmit Card

Digital Card

LPT Mechanical Design

5 WATT HPA

DUAL TX

QUAD RX

HPA PWR SUPPLY

GEN III DIGITAL

I/O
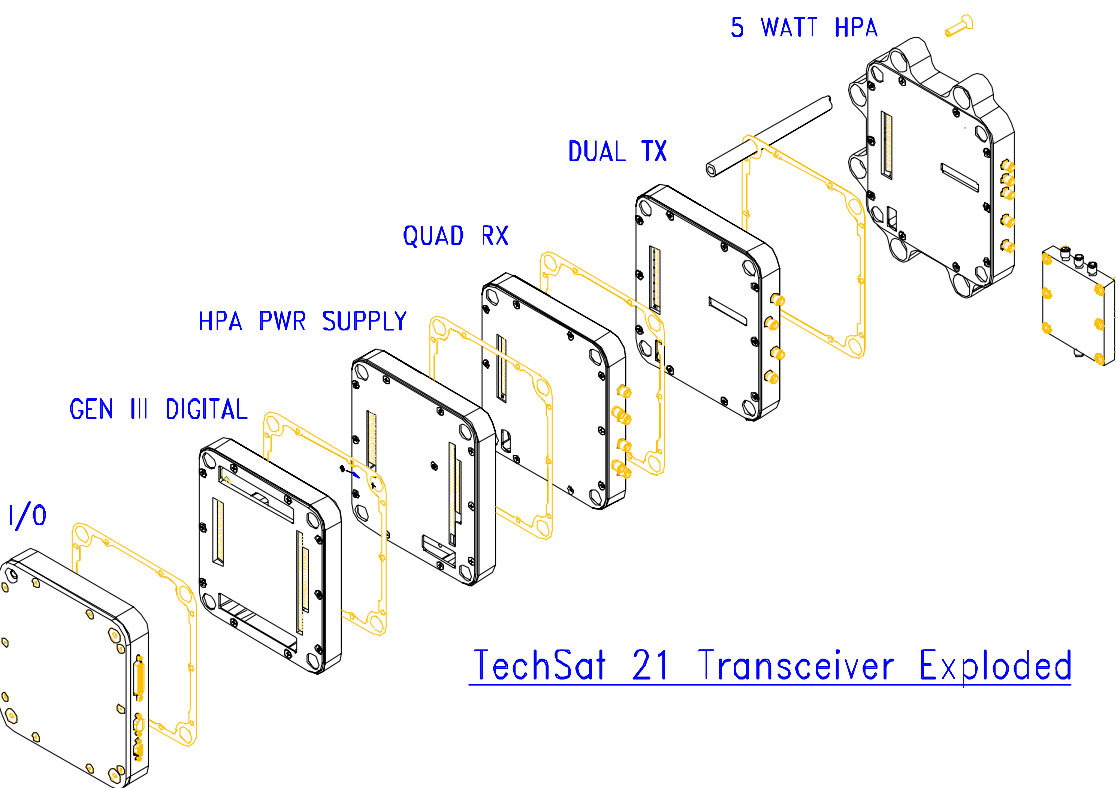
**TechSat 21 Transceiver Exploded**

Mechanical Design Features:
- ❑ **Individual circuit cards rigidly mounted to aluminum "frames"**
- ❑ **Each frame conforms to specific requirements of its CCA**
  - ➢ RF shielding
  - ➢ Connector I/O
  - ➢ Cable routing
- ❑ **Thermally conductive pads placed above and below each CCA for heat transfer**
  - ➢ Additional heat transfer capability provided via PCB thermal planes
- ❑ **Heat plates complete the "frame" assembly**
  - ➢ Provide conductive path from heat pads to external heat sinking
  - ➢ Fitted with EMI gasket to shield CCAs from one-another
  - ➢ Complete assembly provides vibration dampening for each CCA, isolates CCAs from each other
  - ➢ I/O routed either through frame walls or end covers

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LPT Hardware Modules

☐ **In general, a full complement of LPT modules includes:**

- ➤ **Power and I/O Module**
- ➤ **Digital Signal Processing Module**
- ➤ **Dual RF Transmitter Module(s)**
- ➤ **Quad RF Receiver Module(s)**
- ➤ **RF Power Amplifier Module**

☐ **These modules may be combined in various quantities to provide different capabilities, as required.**

- ➤ **Up to four Quad RX Modules may be combined to provide 16 independent RF receive bands**
- ➤ **A second DSP Module may be stacked to increase the number of demodulator channels from 32 to 64 (or higher)**

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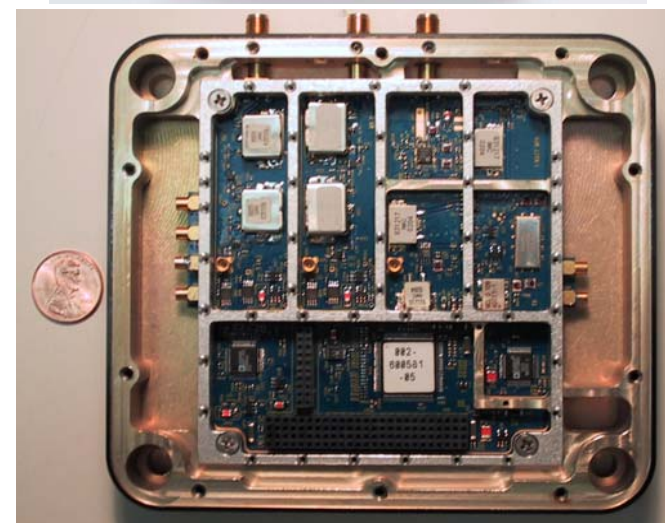
Design of a Radiation-Tolerant LPT (rLPT)

❑ **Goals**

  ➢ **Develop LPT architecture that can be tailored to provide appropriate level of reliability and radiation-tolerance as required by application**

  ➢ **In radiation-tolerant LPT design, maintain most of the LPT's functional capabilities and reprogrammability**

❑ **Approach—address reliability and radiation tolerance of each LPT module independently**

❑ **Key Technologies Areas**

  ➢ **Power supply**

    • **Incorporate existing rad-hard components**

  ➢ **RF hardware**

    • **Inherent immunity of many parts**
    • **Hybrid packaging provides for improved device reliability**
    • **Radiation screening where existing component data is insufficient**

  ➢ **Digital hardware**

    • **Incorporate existing rad-hard components where available**
    • **Ensure latch-up immunity through component selection**
    • **Mitigate/tolerate SEUs in FPGAs, memories, A/Ds and D/As**

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Radiation Mitigation in the Digital Module

❑ **Use radiation-hardened FPGAs to host LPT signal processing**

- ➢ **Xilinx FPGA**
  - • **Size and speed appropriate for LPT signal processing**
  - • **Maintains reconfigurable functionality**
  - • **Fault-tolerant architecture increases FPGA resource requirements**
- ➢ **Actel FPGA**
  - • **Provides robustness for control functions**

❑ **Replace "soft" DSP**

- ➢ **Move select functions to radiation-hardened FPGAs**
  - • **Focus on high duty cycle routines that use significant DSP resources**
  - • **Reduces the capability requirement of the DSP (MIPS, RAM)**
- ➢ **Atmel (Analog Devices) 21020**
  - • **32-bit floating point rather than 16-bit fixed point**
 - • **20 MFLOPs when running at 3.3V**

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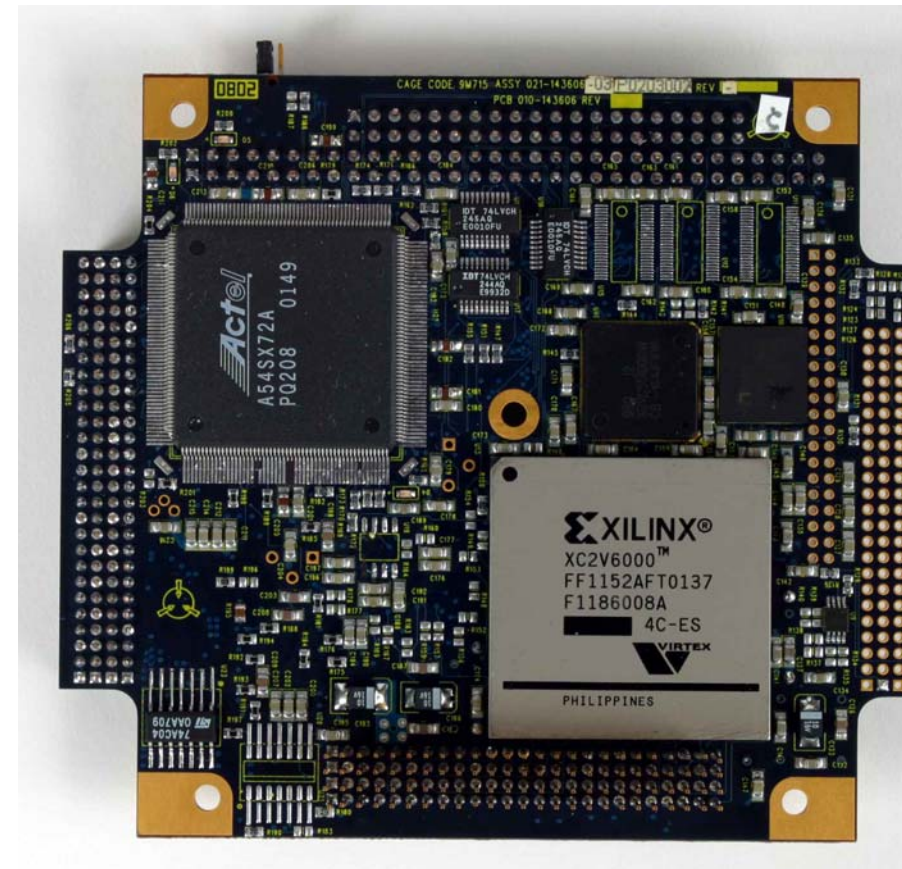
Radiation Effects on Reconfigurable Xilinx FPGAs

❑ **Radiation effects on Xilinx QPRO-plus FPGAs (Virtex)**
  - ➤ **TID immune to >100 krads(Si)**
  - ➤ **SEL immune to 120 MeV-cm^2/mg**
  - ➤ **Susceptible to SEUs (mitigation required)**

❑ **Xilinx FPGA Architecture**
  - ➤ **CLBs, Block RAM, and I/O Blocks**
  - ➤ **Programmable routing resources**
  - ➤ **Flip-flops**
  - ➤ **Clocking resources**
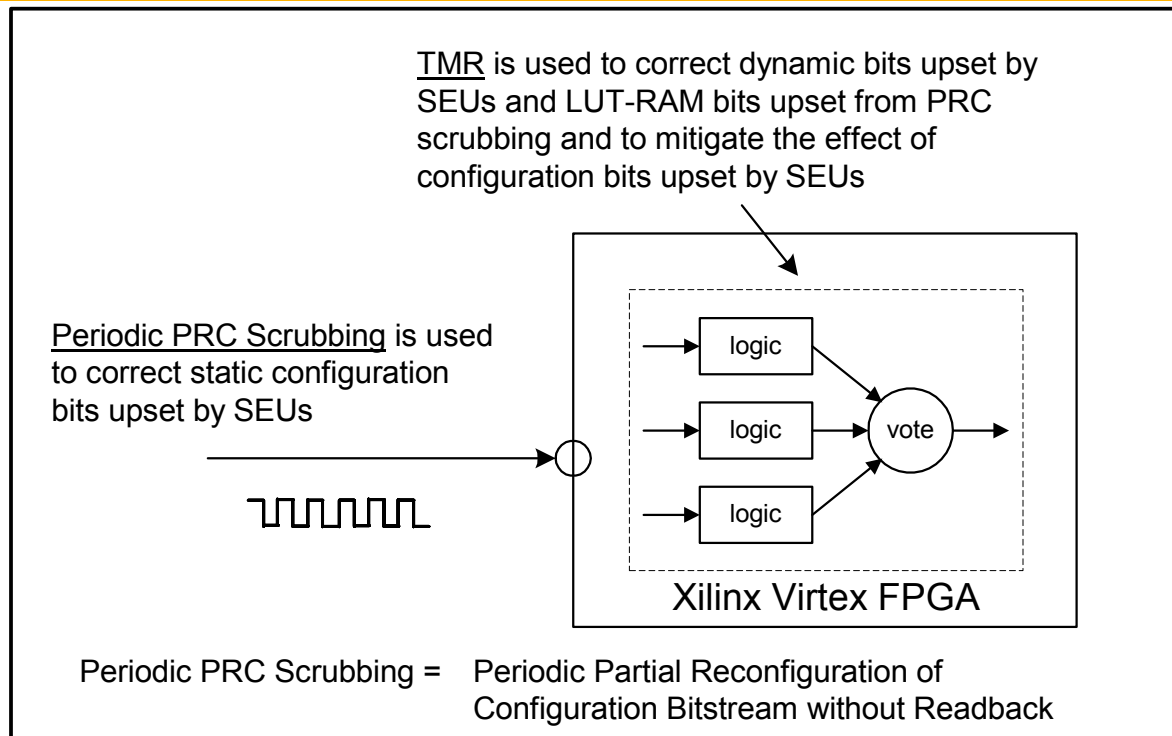 - ➤ **Configuration control logic**
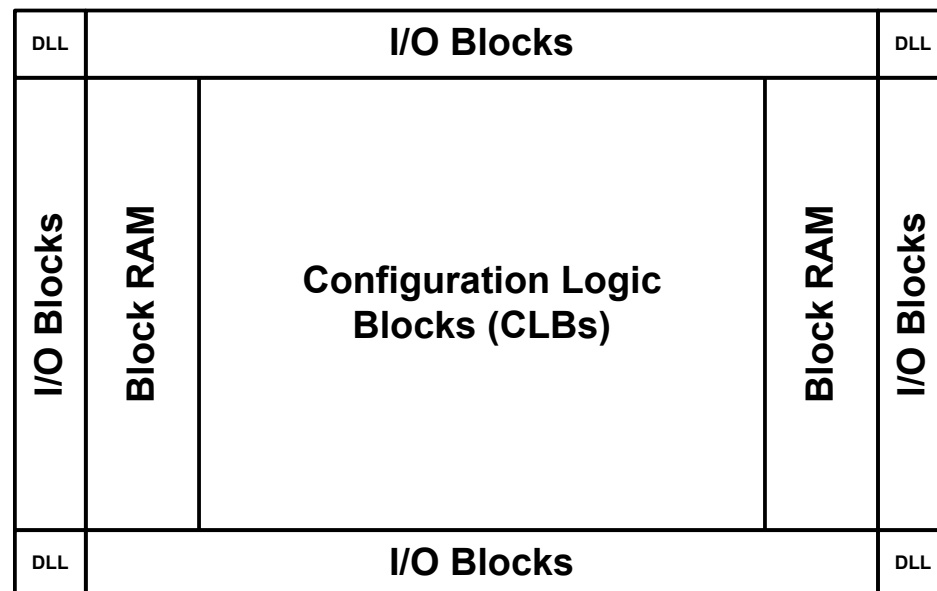
❑ **Types of SEUs**
  - ➤ **Configuration upsets**
  - ➤ **User logic upsets**
  - ➤ **Single event functional interrupts (SEFI)**
  - ➤ **Special feature upsets (Clocking, I/O)**
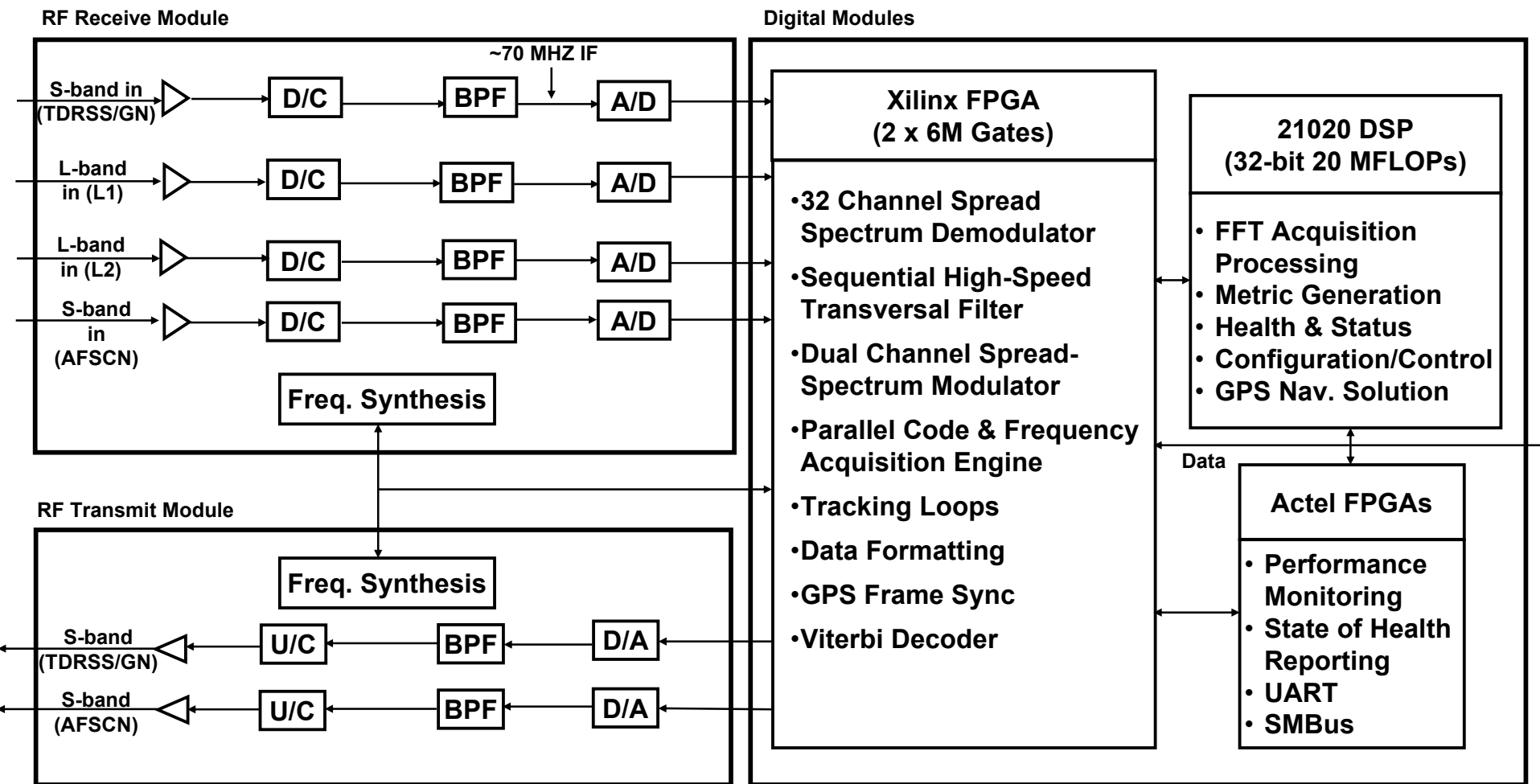 - ➤ **Half-latch upsets**

DLL	I/O Blocks			DLL
I/O Blocks	Block RAM	Configuration Logic Blocks (CLBs)	Block RAM	I/O Blocks
DLL	I/O Blocks			DLL

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SEU Mitigation in Xilinx Virtex FPGAs

TMR is used to correct dynamic bits upset by SEUs and LUT-RAM bits upset from PRC scrubbing and to mitigate the effect of configuration bits upset by SEUs

Periodic PRC Scrubbing is used to correct static configuration bits upset by SEUs

Xilinx Virtex FPGA

Periodic PRC Scrubbing =   Periodic Partial Reconfiguration of Configuration Bitstream without Readback

❑ **SEUs are mitigated with judicious combination of techniques**
  ➢ **Triple-module redundancy (TMR) of FPGA's VHDL code**
  ➢ **Partial reconfiguration (PRC) scrubbing of FPGA bitstream**
  ➢ **Prevent half-latch structures from being used in FPGA design**
  ➢ **Reconfigure/reset FPGA based upon SEFI signature detection**
❑ **Approach has been proven to correct all SEUs in Virtex FPGA**
 ➢ **The only functional upsets are caused by SEFIs**

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Radiation-Tolerant 3rd Generation LPT Architecture

RF Receive Module

Digital Modules

~70 MHZ IF

S-band in (TDRSS/GN) ▷ → D/C → BPF → A/D

L-band in (L1) ▷ → D/C → BPF → A/D

L-band in (L2) ▷ → D/C → BPF → A/D

S-band in (AFSCN) ▷ → D/C → BPF → A/D

Freq. Synthesis

Xilinx FPGA (2 x 6M Gates)

- •32 Channel Spread Spectrum Demodulator
- •Sequential High-Speed Transversal Filter
- •Dual Channel Spread-Spectrum Modulator
- •Parallel Code & Frequency Acquisition Engine
- •Tracking Loops
- •Data Formatting
- •GPS Frame Sync
- •Viterbi Decoder

21020 DSP (32-bit 20 MFLOPs)

- • FFT Acquisition Processing
- • Metric Generation
- • Health & Status
- • Configuration/Control
- • GPS Nav. Solution

Data

Actel FPGAs

- • Performance Monitoring
- • State of Health Reporting
- • UART
- • SMBus

RF Transmit Module

Freq. Synthesis

S-band (TDRSS/GN) ◁ ← U/C ← BPF ← D/A

S-band (AFSCN) ◁ ← U/C ← BPF ← D/A
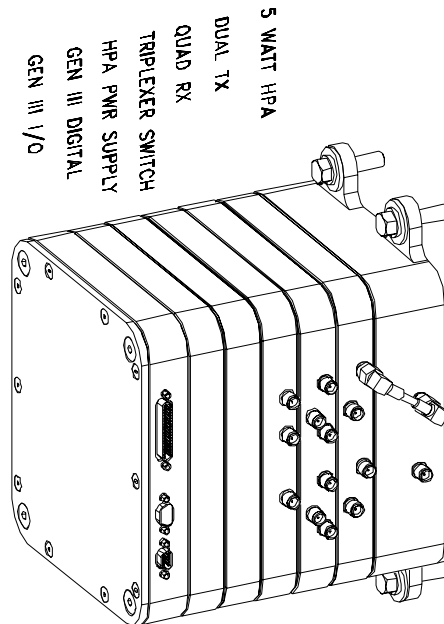
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Application of the LPT in Space

❑ **CANDOS (NASA)—2003**

  ➢ **Successful demonstration of communication and navigation functions on STS-107 in Jan. 2003**
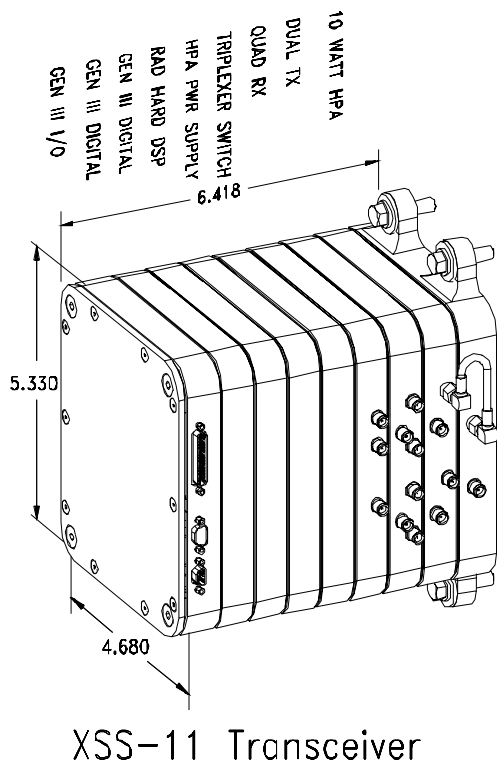
XSS-11 Transceiver
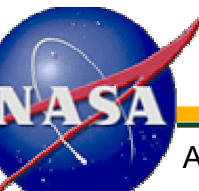
❑ **XSS-11 (AFRL)—2004**

  ➢ **Provide communication & navigation functions on one-year mission in 2004**

TechSat 21 Transceiver

❑ **TechSat 21 (AFRL)—TBD**

 ➢ **Provide communication & navigation functions on one-year flight**

CANDOS Experiment Overview

- ❑ **Communications and Navigation Demonstrations On Shuttle (CANDOS) was flown on Space Shuttle Columbia's STS-107 mission in January 2003**
  - ➤ **First application of LPT in space—complete success**
  - ➤ **Experiment included LPT, three S-band antennas, and one L-band antenna mounted to Hitchhiker cross-bay bridge**
  - ➤ **Interfaces with Hitchhiker power and avionics for asynchronous uplink/downlink "lifeline" and Shuttle crew panel switches**

- ❑ **On-Orbit Experiments/Demonstrations**
  - ➤ **Simultaneous communications and navigation**
    - • **Mobile-IP via TDRSS and GN for all communications**
    - • **NASA GSFC GPS Enhanced Orbit Determination Experiment (GEODE) software for autonomous orbit determination**
  - ➤ **On-orbit reconfiguration of signal processing engine**

- ❑ **On-Orbit Measurements/Processing**
  - ➤ **GN/SN link quality**
  - ➤ **Receiver performance (e.g., acquisition speed, number of simultaneous tracked signals)**
  - ➤ **GPS observables (e.g., pseuodorange, Doppler, time estimates)**
  - **GPS position/velocity/time estimation and Shuttle orbit determination**

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CANDOS on Hitchhiker

LPT

SOLCON

SOLSE

MEIDEX

MPESS

FORWARD

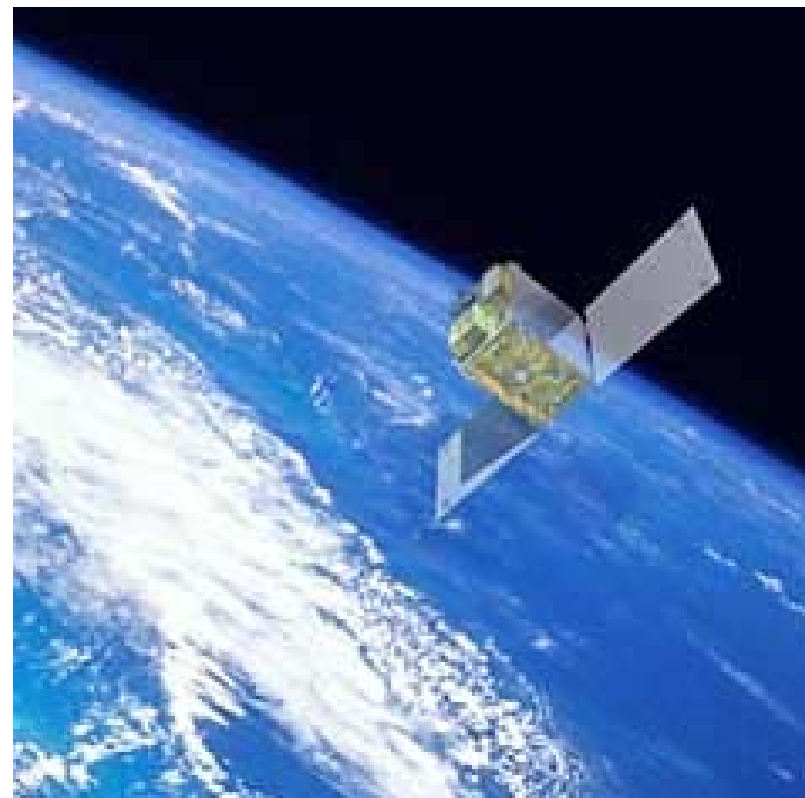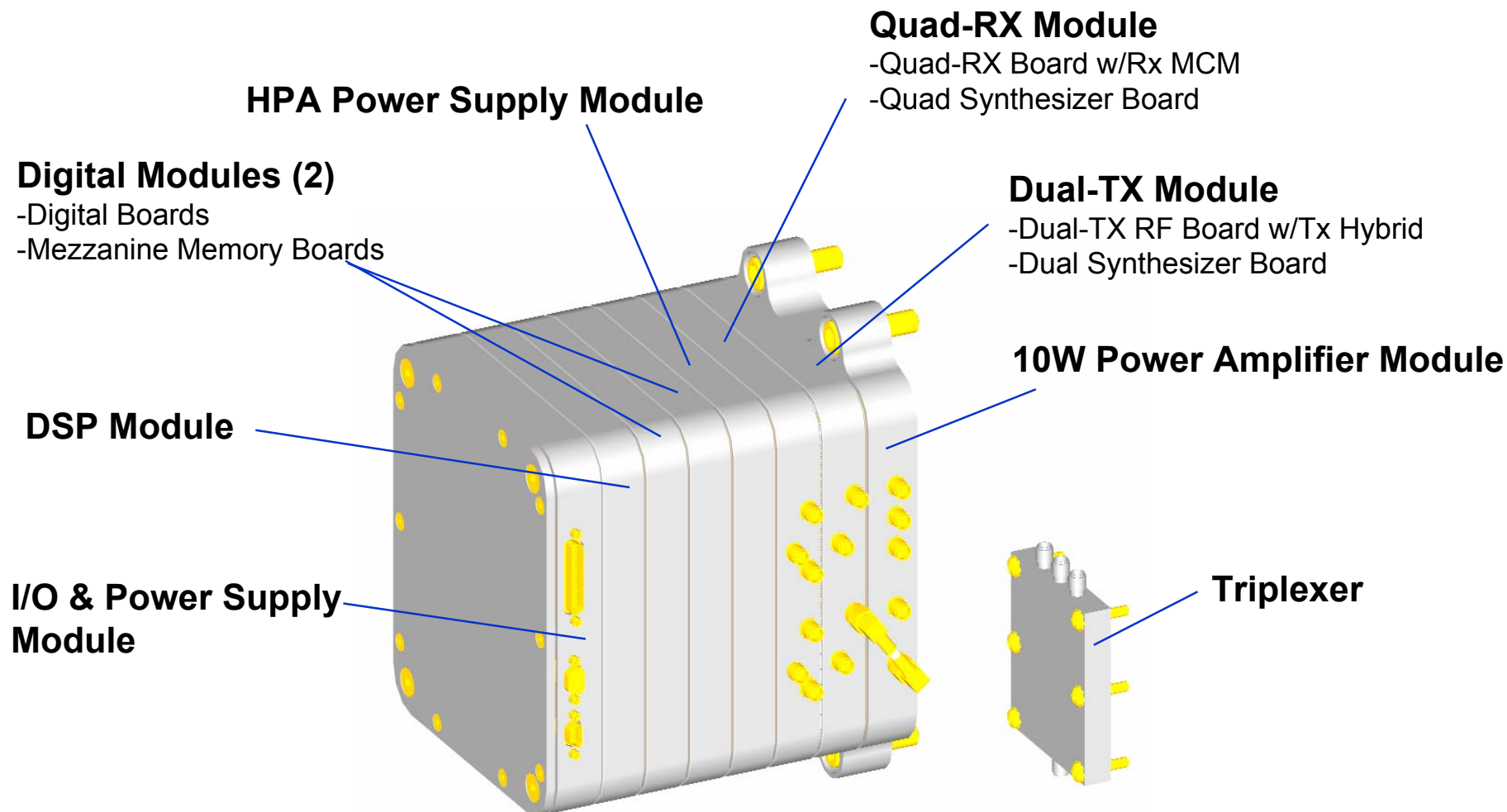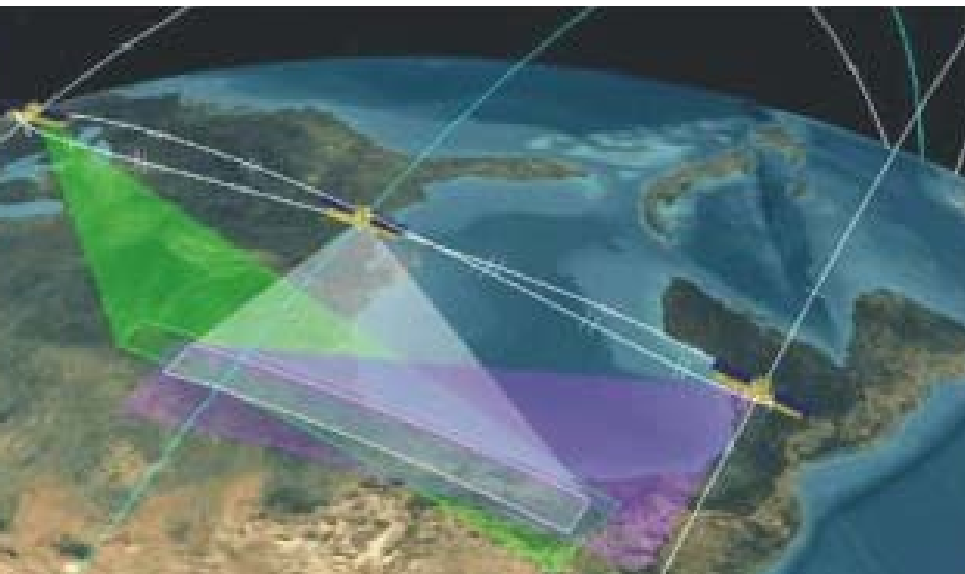ITT Industries
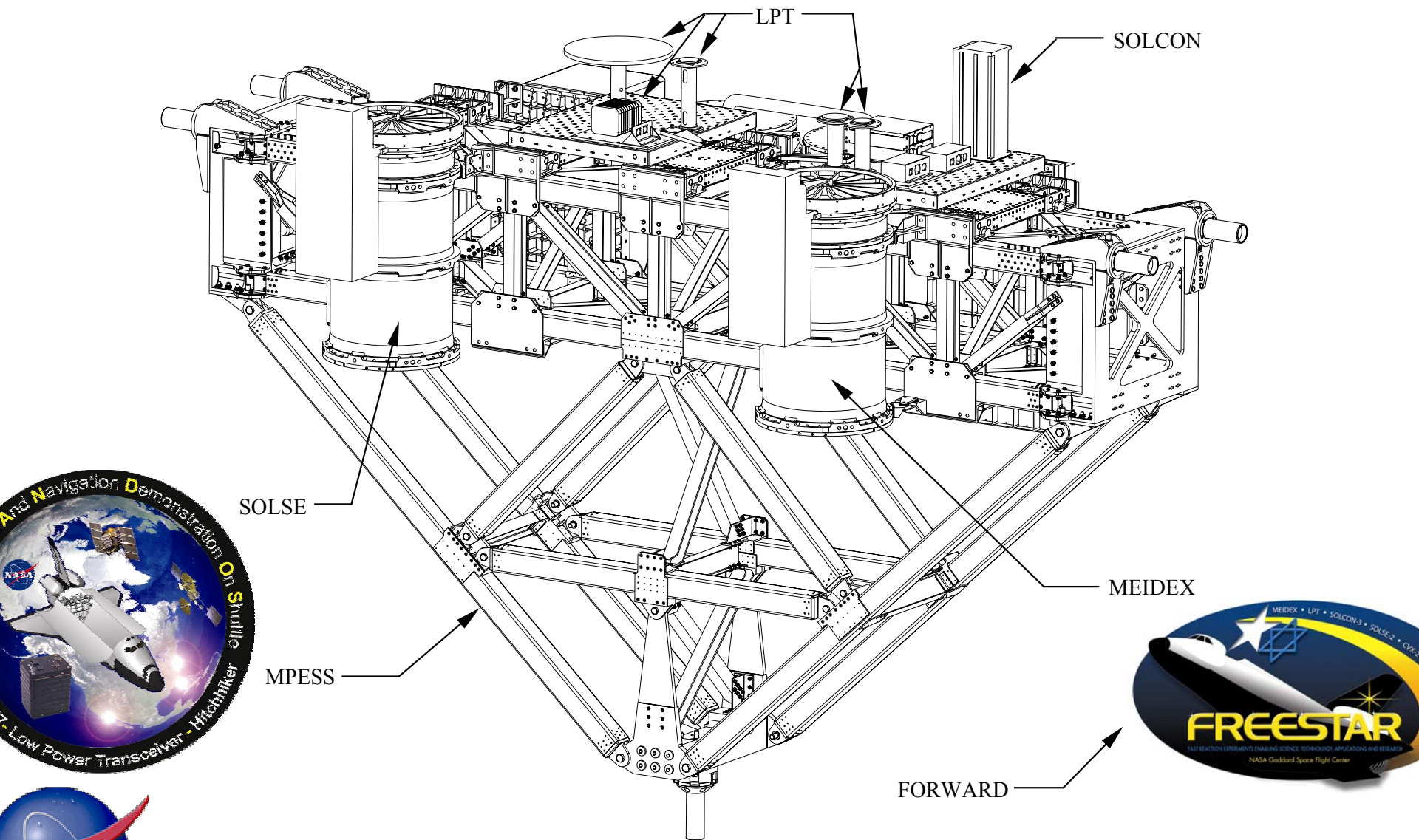
LPT on XSS-11

❑ **LPT will be the primary TT&C transceiver and GPS receiver for AFRL's XSS-11 satellite**

   ➢ **Satellite integrated by Lockheed-Martin Astronautics**

   ➢ **One-year mission scheduled for 2004**

❑ **LPT Functions for XSS-11**

   ➢ **Full-duplex communications via the AFSCN, TDRSS, or STDN**

      • **Demonstrates "unified S-Band" (USB) capability**

   ➢ **Paired with an external COMSEC device to provide secure TT&C for the spacecraft**

   ➢ **Integrated GPS signal reception and orbit determination using L1 (C/A) as well as the new civil signal on L2 (L2C)**

   ➢ **Reconfigurable system**

      • **Demonstration of on-orbit firmware upload that will track L2 civilian code**

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XSS-11 LPT Configuration

Quad-RX Module
-Quad-RX Board w/Rx MCM
-Quad Synthesizer Board

HPA Power Supply Module

Digital Modules (2)
-Digital Boards
-Mezzanine Memory Boards

Dual-TX Module
-Dual-TX RF Board w/Tx Hybrid
-Dual Synthesizer Board

10W Power Amplifier Module

DSP Module

I/O & Power Supply Module

Triplexer

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LPT on TechSat 21*

❑ **LPT is targeted to be the primary TT&C transceiver and GPS receiver for AFRL's TechSat 21 formation flying experiment**

  ➢ **Integrated by MicroSat Systems, Inc.**
  ➢ **Three identical spacecraft**
  ➢ **One-year mission**
  ➢ **Demonstrate spacecraft cluster operations and synthetic aperture RADAR**

❑ **LPT Functions for TechSat 21**

  ➢ **Full-duplex communications via the AFSCN**
  ➢ **Paired with an external COMSEC device to provide secure TT&C for the spacecraft**
  ➢ **Half-duplex satellite crosslink**
    • **Provides high speed data link between spacecraft**
    • **Incorporates a CDMA-based ranging capability**
  ➢ **Integrated GPS signal reception and orbit determination using L1 (C/A)**

*status of mission currently on hold

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TechSat 21 Navigation

❑ **The TechSat 21 spacecraft program provides a difficult navigation challenge: real-time GPS-based relative navigation for spacecraft separations from many kilometers down to 10's of meters**

> ➢ **Due to the flight-critical nature of the navigation functions, the LPT's navigation software is hosted on the spacecraft's radiation hardened processor rather than internal to the LPT**

❑ **Navigation functions include:**

> ➢ **GPS satellite tracking assignment**
> ➢ **Point position solution**
> ➢ **GEODE**
> ➢ **Relative navigation filter (RELNAV)**

❑ **LPT relative navigation performance:**

> ➢ **Position: 10's of cm**
> ➢ **Velocity: sub-mm/s**
> ➢ **Clock offset: 10's of nanoseconds**

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The Future of LPT

❑ **Future developments rely upon application of continued advances in COTS component technology**

  ➢ **Develop RF frequency agility for RX and TX paths**

   • **Use high-speed ADCs, DACs, and FPGAs**

  ➢ **Increase signal processing capacity and speed**

   • **Exploit increased speed and density of ADCs, DACs, and reconfigurable FPGAs/DSPs**

  ➢ **Decrease in power consumption and device size**

   • **Power supplies**

   • **Analog and digital components**

   • **Discretes**

❑ **The Miniature Transceiver (MinT)**

  ➢ **Reduce volume by an order of magnitude from ~100 cubic inches to ~10 cubic inches**

  ➢ **Expanded signal processing capabilities through use of next generation FPGAs and DSP**

  ➢ **Targeting reconfigurable space applications (e.g., nano-satellites) as well as other platforms (aircraft, terrestrial uses)**

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Conclusion

Low Power Transceiver (LPT)
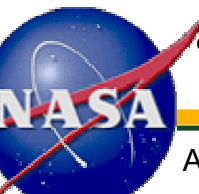
❑ **The LPT is revolutionizing the state-of-the-art in spacecraft communications and navigation technology**

❑ **The 3rd Generation rLPT will meet the reliability needs of current and future space applications**

❑ **The CANDOS experiment, XSS-11, and TechSat 21 demonstrated/will demonstrate the capabilities of the LPT in a space environment**

❑ **Future evolutions will continue to reduce the power, mass and volume requirements of the LPT in order to enable more cost effective missions**

4.68"

2.99"

5.33"

Relay Satellite

Comm & Ranging

Comm & Ranging

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